

# MOS FIELD EFFECT TRANSISTOR 2SK3484

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SK3484 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

#### FEATURES

- Low On-State Resistance  
 $R_{DS(on)1} = 110 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 8 \text{ A)}$   
 $R_{DS(on)2} = 125 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 8 \text{ A)}$
- Low  $C_{iss}$  :  $C_{iss} = 930 \text{ pF TYP.}$
- Built-in Gate Protection Diode
- TO-251/TO-252 package

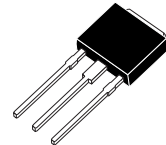
#### ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3484	TO-251
2SK3484-Z	TO-252

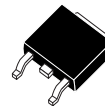
#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	100	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 16$	A
Drain Current (Pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 64$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_T$	30	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_T$	1.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	T.B.D. <sup>Note3</sup>	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	T.B.D. <sup>Note3</sup>	mJ

(TO-251)



(TO-252)



**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

**3.** T.B.D. : To be determined

#### THERMAL RESISTANCE

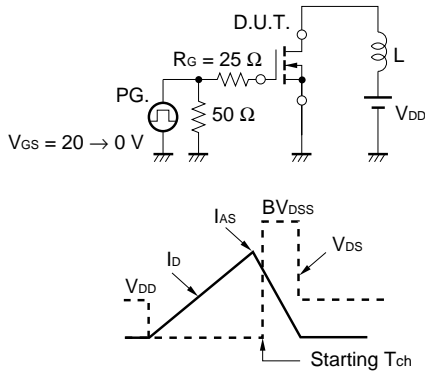
Channel to Case	$R_{th(ch-C)}$	4.17	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.  
 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

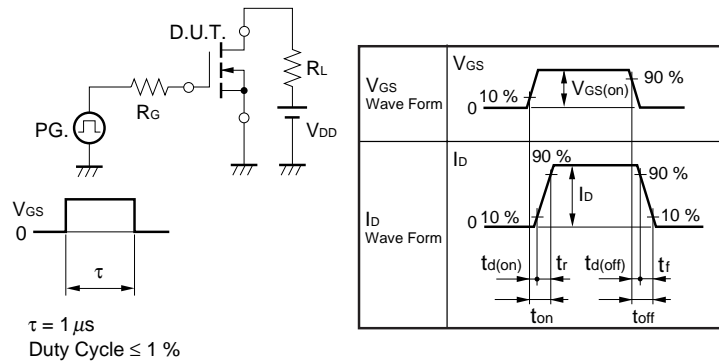
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8 A		85	110	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 8 A		93	125	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 8 A	10	20		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		930		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		90		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		50		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 8 A		10		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		6.0		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 50 V		35		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 1 Ω		5.0		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 16 A		17		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 80 V		3.0		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS(on)</sub> = 10 V		5.0		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 16 A, V <sub>GS</sub> = 0 V		1.0		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 16 A, V <sub>GS</sub> = 0 V		85		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		160		nC

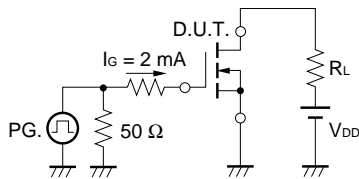
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

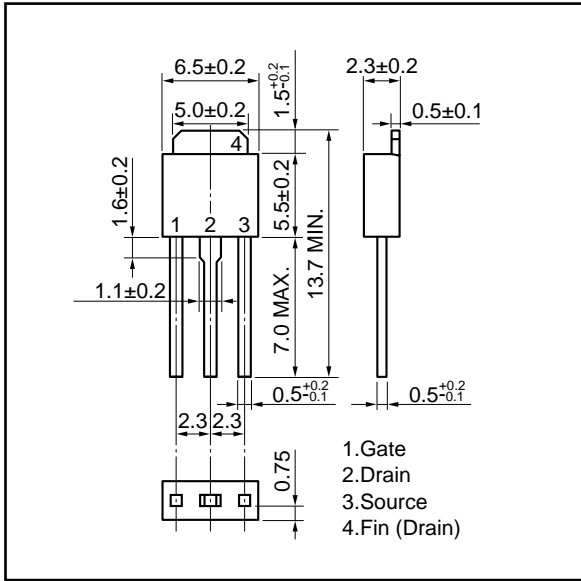


**TEST CIRCUIT 3 GATE CHARGE**

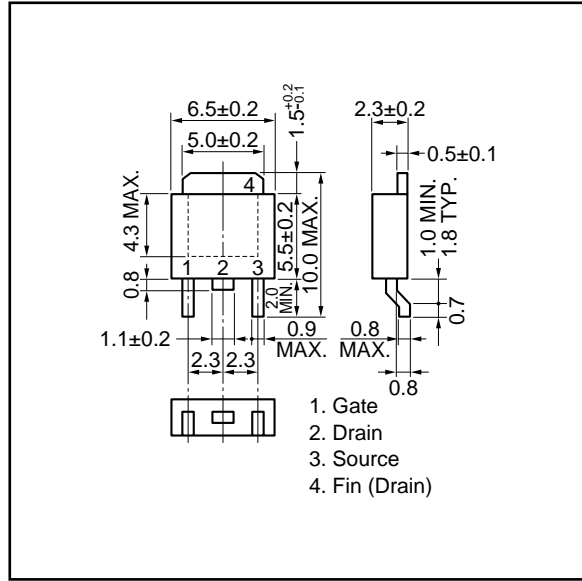


PACKAGE DRAWINGS (Unit : mm)

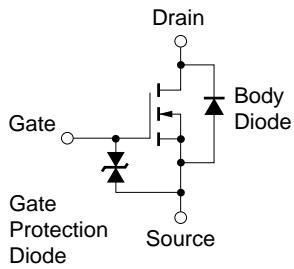
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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